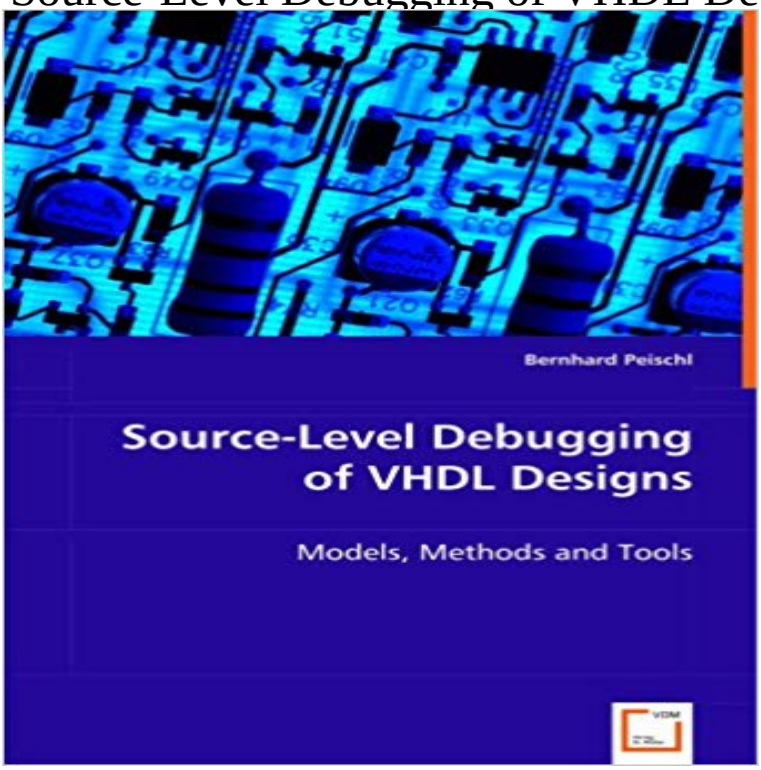
Source-Level Debugging of VHDL Designs: Models, Methods and Tools



As design density and complexity of digital systems increase, the costs due to design faultsincrease exponentially. Therefore, detecting, localizing, and correcting faults are crucial issuesin today`s fast-paced and fault-prone development process. Test case generation and verificationtools detect faults and provide the user with a failing run. Even with a detailed failing run inhand, locating and correcting a fault is a bland and time-consuming chore.Debugging, which is the process of locating and correcting a fault, is not done solely bydesigners. The verification engineers, the ones who write and run the verification tests, usuallyspend quite a lot of their own time analyzing the failure traces themselves. Debugging is one of the most time consuming tasks in the effort to improvesystem quality. It takes 50 to 80 percent of the time used for verification depending on the levelof automation of the verification tools. Fault localization may significantly reduce design cycletime by reducing the overall debugging time.This book focuses on models, methods, and techniques for the design and development of debugging tools and specifically addresses verification engineers.

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